

Market Participants' note on the application of Individual Validation Adjustments (IVAs)

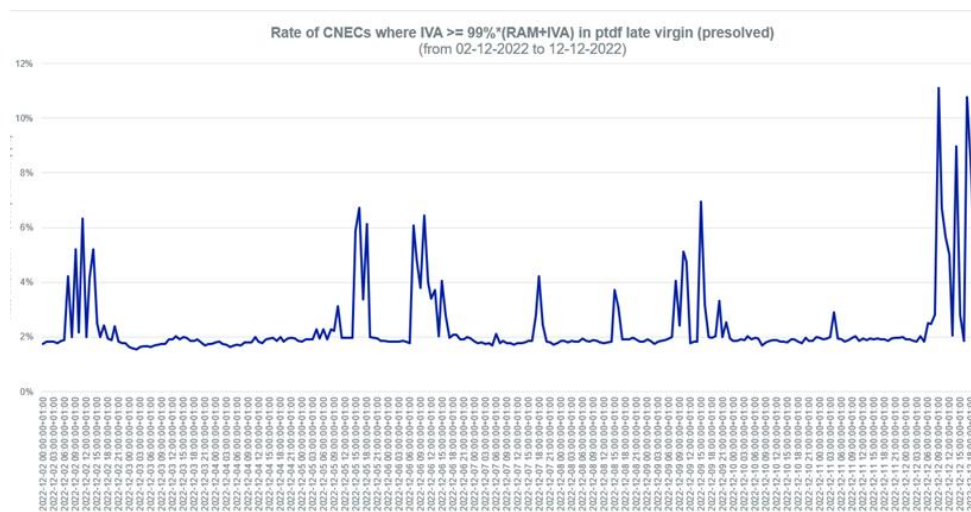
22 December 2022, Brussels

Object: (1) Expression of concerns about pre-congested flow-based domains in Core, mainly linked to IVAs, (2) request for clarification of IVA processes (in particular with DaVinci TSOs and Transelectrica) and (3) enactment of possible improvements

Since Core go live, there have been many occurrences of TSOs applying bulk reductions to the margins of their CNECs before market coupling through IVAs. This is sometimes done to the point where several elements can be left with virtually no RAM, particularly in the control areas of DaVinci TSOs (AT, DE, NL) and Transelectrica (RO).

This issue was already raised by Market Participants during the external parallel runs where some of the Flow-Based domains were even published empty (no exchange possible). Although the situation has improved, the current usage of IVAs is still leading to significant domain reductions on a recurrent basis.

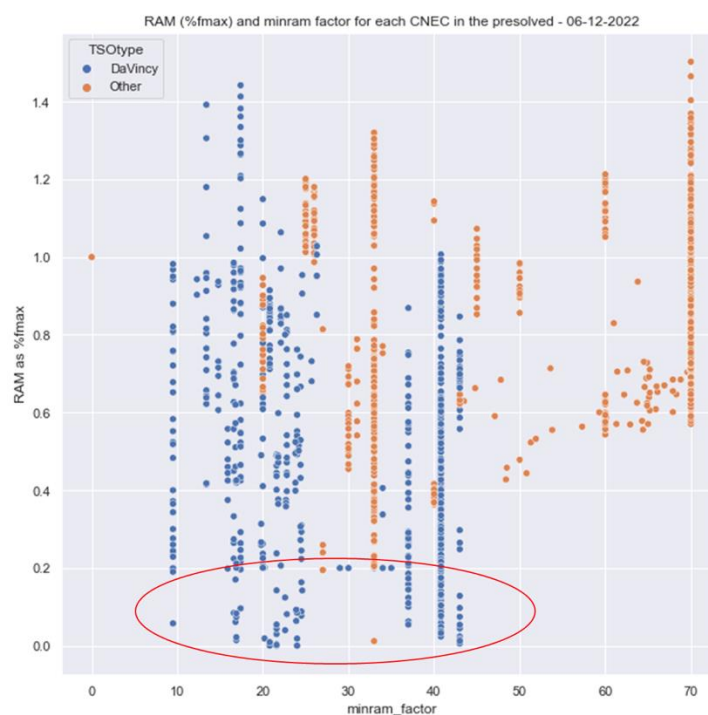
According to article 20(5) of the Core DA CCM, RAMs shall only be reduced by IVA to the “minimum degree that is needed”. While we support and understand the need for TSOs to ensure grid security, the IVAs of DaVinci TSOs in particular, seem to recurrently curtail some RAMs in full, with validations sometimes above 100% of Fmax. In our view, this is not in line with a reasoned utilization of the IVA lever, and the justifications provided are too succinct. Besides, it also breaches the 20% min RAM legal threshold required by Article 17(7) of the Core DA CCM.



Although the chart is recent, the problem is not. ‘DaVinci’ was initiated to reduce the volume of IVA applied (compared to having only individual assessments from concerned TSOs), however in reality it

is the largest producer of such reductions. As already pointed out by the CREG [in their study](#): “the occurrence of such violations is neither exceptional nor strictly limited to what is necessary for operational security”. In addition, the use of ‘Da Vinci’ process to solve overloads on internal network elements that are not necessarily part of the set of critical network elements is highly questionable, as also pointed out in the CREG study.

More in general, the issue of low RAM available on Critical Network Elements is frequently observed. As an example, we refer to the delivery date December 6th 2022 where an extremely high number of CNECs with RAM below 20% were present. The ACER decision on CORE CCM is however stating that this kind of situation should remain exceptional.



As market conditions are tightening going into the colder winter, these pre-congested Flow-Based domains have recently led to large price divergence and welfare reduction as bid-ask curves become very steep. In annex, you will find graphs highlighting the situation of repeated min RAM at 0, apparently linked to significant IVAs, during the first half of December 2022.

We therefore urge the TSOs to take action as follows:

- Provide full transparency on their IVA processes (full methodology). This is both a matter of disclosing the methodologies employed upstream (official requirement of the [Core CACM package](#)) but also improving the quality of the downstream messaging service. The current format remains too unclear, full of “N/A” and does not always inform of the specific reason for the reduction (examples in the annex).

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- Moderate interventions in their IVA process to what is strictly necessary to ensure operational security according to article 20(5) of the Core DA CCM.
- Clarify the usage of validation process on network elements that are not part of the set of critical network elements.
- Guarantee the 20% minimum RAM on all CNECs according to article 17(7) of the Core DA CCM.
- If necessary, enact improvements in their IVA processes to ensure the respect of the two rules above
- Provide fully detailed justification for any breach of the two rules above

